Source Mask Optimization Methodology (SMO) & Application to Real Full Chip Optical Proximity Correction

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ABSTRACT

Due to the continuous shrinking in half pitch and critical dimension (CD) in wafer processing, maintaining a reasonable process window such as depth of focus (DOF) & exposure latitude (EL) becomes very challenging. With the source mask optimization (SMO) methodology, the lithography process window can be improved and a smaller mask error enhancement factor (MEEF) can be achieved.

In this paper, the Tachyon SMO work flow and methodology was evaluated. The optimum source was achieved through evaluation of the critical designs with Tachyon SMO software and the simulated performance was then verified on another test case. Criteria such as DOF, EL & MEEF were used to determine the optimum source achieved from the evaluation. Furthermore, the process variation band (PV-Band) and the number of hot spot (design weak points) were compared between the POR and the optimum source. The simulation result shows the DOF, MEEF & worst PV-Band were improved by 13%, 17% & 12%, respectively with the optimum SMO source.

In order to verify the improvement from the optimum SMO at the silicon level, a new OPC model was recalibrated with wafer CD from the optimized source. The OPC recipe was also optimized and a reticle was retrofitted with the new OPC. By comparing the process window, hotspots and defects between the original vs. new reticle, the benefit of the optimized source was verified on silicon.

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Keywords: SMO, Freeform, Process window, MEEF, PV-Band, Full chip, OPC, Pattern selection

1. INTRODUCTION

Source mask co-optimization (SMO) [1-4] has become one of the key enablers for the continuation of scaling of design rules in critical layers of 2x nodes and beyond using ArF lithography [5-6]. GLOBALFOUNDRIES has worked on the SMO approach for several years and some achievements have already been published [7-8]. The requirement that the optimized source from SMO can be applied to the full-chip layout demands that as many clips as possible need to be included in the optimization. This is to ensure the resulting source is optimal for all pattern varieties and pitches for the layer of interest. However, SMO is highly computational intensive, which puts an upper limit on the total clip areas and number of clips that can be included in a SMO run for a reasonable turn-around time.

In this paper, we present a full-chip SMO flow, which integrates SMO with full-chip correction and verification tools to address the compromise between lithographic performance and turnaround time. One of the most critical elements in this flow is a diffraction-based pattern selection algorithm developed to select the most critical patterns for source

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optimization. This significantly reduces the SMO runtime to find the optimized source by only including patterns that are most source-critical or sensitive. To demonstrate how this flow was applied in a realistic full-chip application, a real 28 nm dark field layer was used as an example. For this study, patterns of different coverage scopes were categorized into class A and B, each including about 100 and 500 clips, respectively. Device C and D of larger coverage were used for verification. A process of record (POR) source was used as a comparison. The final result was verified experimentally on wafers.

The paper is organized as follows. Section two introduces the full-chip SMO flow, in particular the diffraction-based pattern selection method for source optimization and how it applies in this study using Class A clips. Section three applies the full-chip SMO flow on the 28 nm dark field layer and shows the simulated results with the optimized source compared with the POR source. Wafer verification and process window comparison between the SMO and POR sources is discussed in section four.

2. METHODOLOGY

2.1 Full chip SMO methodology

The full-chip SMO flow is shown in Figure 1. The goal of this flow is to generate a source that produces superior lithographic performance compared with an existing POR process within a reasonable turnaround time. To achieve this, the flow proceeds iteratively between two major blocks: source optimization with SMO and pattern selection, and full-clip verification of the SMO result with full-clip correction and verification tools, e.g., OPC with model-based sub-resolution assist feature (MB-SRAF) and lithography manufacturability check (LMC). The iterative flow exists to ensure full coverage but in this exploration this was not needed and didn't occur.

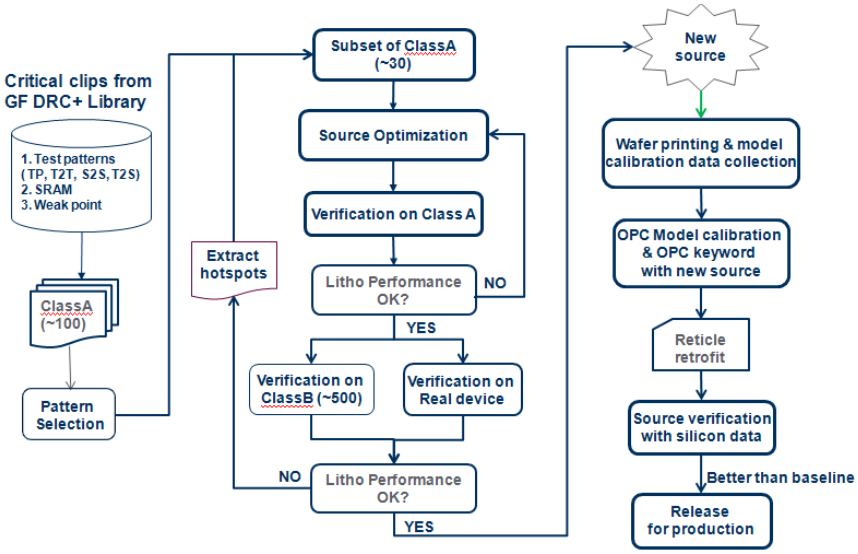


Figure 1 Full-chip SMO Work Flow

The first step of the flow requires pattern preparation for source optimization and verification of the full design set, respectively. Since SMO cannot be directly applied on a full chip design, it was necessary to first prepare a set of patterns for source optimization. These patterns need to cover the full proximity range. Pattern types included critical memory cells, based on the design rules representative of the design set. It was possible to also include known lithography hot spots based on prior understanding of the design rules. The end result of this initial screening of representative clips from the full chip layout was about 100-1000 clips for source optimization. A larger set of clips with more variation of the design rule combinations and warm spots comprise the set of clips for full chip verification.

In this study, several sets of clips were generated from GLOBALFOUNDRIES' DRC library. The first set of clips, or Class A clips, consists of 112 most critical clips, including SRAM, test patterns and hot-spot clips selected based on hot-spot analysis with the POR process. A more extensive set of class B clips includes over 500 clips with more design rule variations and warm spots. Class A was a subset of class B clips. In this study, Class A clips were used for source optimization, while class B was used for SMO result verification. Two more large-area devices C and D were used for verification. The largest of all was device D with an area of 790 * 90 um.

With the patterns ready, the flow starts with the source optimization block (Figure 1). Since the input 100-1000 clips were still too computationally expensive for SMO, we need to further reduce the number of clips to a much smaller fraction for source optimization. The diffraction-based pattern selection tool was used to find out which clips were most critical for source optimization. Typically this is able to reduce the number of clips for SMO to 20-50 clips based on the pattern complexity and degeneracy which can reduce the SMO runtime by as much as ~90% in some cases, without sacrificing the final lithographic performance of the optimum source. It is worth noting that this pattern selection method was not intended to select the design hot spots, but rather to select those most source-critical clips. More details and examples of pattern selection will be given in the next subsection.

In this case, with pattern selection, we were able to reduce 112 Class A clips by 76% into 27 clips. Then SMO was run on these selected 27 clips to get the optimum source, and subsequently a mask-only optimization was then run on all Class A clips. The final optimization result of Class A clips was verified using lithography manufacturability check (LMC) to confirm that the solution with the optimized source meets the specification. In the tuning loop shown in figure 1, SMO results may require fine tuning if LMC verification identifies that the new source does not meet the specification. In this experiment the tuning loop was not required, a key proof point in the validity of the pattern selection.

After the SMO solution was verified with the Class A clips, the SMO output model with the optimum source was then used to run full chip OPC with model-based SRAF on all the verification clips, which in this case, were Class B clips and device C and D. Then LMC was run to check if the OPC result met the lithographic spec, and moreover in this case, how it compared with the POR source. As before if the result do not meet the spec, the user can feedback these additional hot spot areas back into the source tuning set of clips and redo the source optimization. However, it is very important to carefully analyze the OPC results, and confirm that the new hot spots are not local design hot spots or due to under-performing OPC. For the former, limited improvements can be achieved with source optimization for local design hot spots like tight line-ends, slivers, or short elbows. Resolving these hot spots requires design optimization or retargeting.

In this study, since Class A clips provided good coverage of all the design rules, pattern types, and known critical lithography hot spots, no second iteration of SMO was necessary. The optimum source from the algorithmically selected 27 clips yields superior performance over POR source on all verification patterns studied.

2.2 Pattern selection

Before introducing the pattern selection method, we first clarify that the objective of such a pattern selection method is to find an optimum source for a large number of clips through optimization on a smaller subset. This is different from lithographic hot spot identification and selection. Pattern selection for source optimization does not necessarily select all the litho-hot-spots, if they are not critical for source optimization. In particular, it is important to note that 1) whether a location is a hot spot or not heavily depends on the choice of the illuminator; 2) a non-process-window-limiting clip in POR may be selected for SMO if it contains a unique pitch component; 3) a local hot spot may not be selected if it does not correspond to a unique diffraction signature, and thus cannot be effectively improved by illuminator optimization.

In light of the unique requirement of the SMO pattern selection, Brion developed a diffraction-based algorithm. This algorithm does not require initial illuminator, post-OPC mask or prior knowledge of lithography hot spots, though still allows user-selected clips as part of the selection condition. Pattern selection for SMO first generates the diffraction order map for all the clips, then analyzes these diffraction orders, and finds the critical pitch components that are not harmonics of other pitches. Based on this information, a coverage relationship among the input clips can be constructed so that a subset of critical clips for SMO can be selected.

Take a simple example of two 1D clips of pitch 80 and 240 nm and CD 40 nm. Only the 1st order of the 80 nm pitch line/space can be captured inside the pupil, while three diffraction orders of the 240 nm pitch are inside the pupil. By identifying the 1st order of 80-nm-pitch overlapping with 3rd order of the 240-nm-pitch clip, the algorithm finds the harmonic relationship of the two principle pitch components, and the clip with the highest sigma or smallest pitch is

selected, while the other clip is considered degenerate, and thus not selected. In this simple example, the choice of selection is apparent from the lithography point of view. The optimum dipole source should have the sigma center match the 1st order of the 80-nm-pitch clip, and two SRAFs should be placed in 240-nm-pitch clip so that the amplitude of the 3rd order is enhanced matching the 1st order of the other clip. This yields the best NILS and iso-focal Bossung curve for the critical 80-nm-pitch clip, without sacrificing the performance of the other clip. It is worth noting that it is not the patterns with the most diffraction orders (i.e. the 240-nm-pitch clip) that are selected, but those with the most critical orders which are selected. For more complex 2D clips, pattern selection analyzes their diffraction orders and relationships similarly, and finds the most critical diffraction orders and clips thereof.

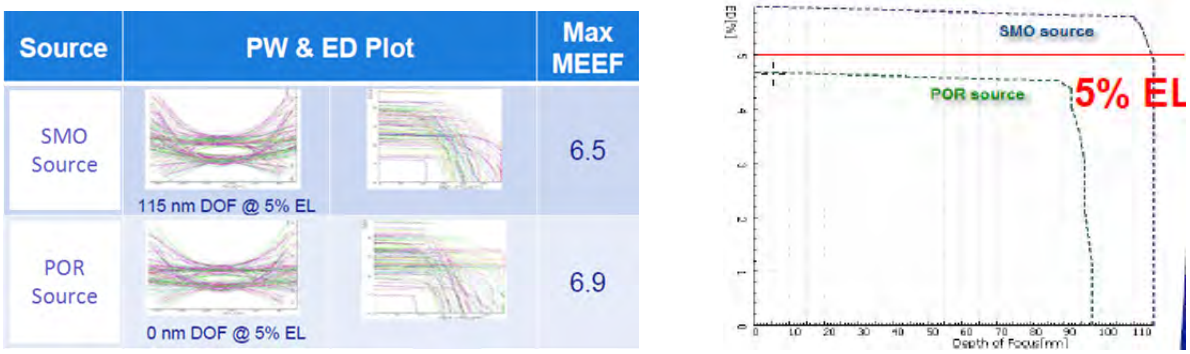
In this study, 112 Class A clips were input into pattern selection for SMO. Among these clips, there were 93 bi-directional test patterns, 1 SRAM cell, and 18 random logic hot-spot clips. The test patterns represent the key design rules from the GLOBALFOUNDRIES 28 nm DRC library, and included lines and spaces with minimum pitch of 90 nm and different types of dense and isolated line-ends. The random logic hot-spot clips were selected from the POR process, and set as preselected. The pattern selection result includes 27 clips, with 8 test patterns, 1 SRAM cells, and all 18 random logic clips. The verification of the pattern selection result will be shown in the next section.

3. SIMULATION

3.1 SMO Source optimization with Class A

Class A was prepared for the input of source optimization based on 112 clips, including the through pitch, line end, SRAM and ORC weak point pattern. After pattern selection, only 27 clips were selected to perform the source optimization. With the Tachyon SMO-MO flow, the optimized SMO source was achieved.

To understand the benefit achieved by the SMO source, a comparison was made using the POR source with the same set of Class A and cut lines, shown in Figure 2. The SMO source showed an improved process window in all measures, DOF, EL and MEEF. The DOF was based on 10% CD variation with the simulation on the cut-line CD. With the SMO source, 115nm DOF @5% EL & 10% CD variation was achieved and the Max MEEF was 6.5, while the POR source had only 0nm DOF @5% EL& 10% CD variation and Max MEEF was 6.9.



(a) (b)

Figure 2. Process window comparison between POR source & SMO source with SMO-Mask Optimization OPC

With the full set of Class A, the SMO source & the POR source with the POR OPC were performed and the process window characterization was done based on LMC/ORC check. The results are shown in Figure 3. With the SMO source, 144 nm DOF was achieved compared with 124 nm DOF for the POR source, which improved by 16.1%. The worst MEEF for SMO source was 9.83, which was improved by 8.3% compared with POR source. The DOF in the LMC process window analysis was based on LMC necking and bridging spec, not the 10% CDV on cutline simulation. For this experiment, the LMC necking and bridging spec was 33 nm & 35 nm, respectively. And the LMC settings for the SMO and the POR source were exactly same for fair comparison. With this test case, we verified two things. 1) Even using the standard OPC production flow the performance was improved with the new SMO source; 2) The pattern selection algorithm was proven to reduce the number of patterns without compromising the process window performance.

Source	SRAF	Mask	DOF @ 5% EL	Worst MEEF
POR	Rule based SRAF	POR OPC recipe	124 nm	10.72
SMO			144 nm	9.83

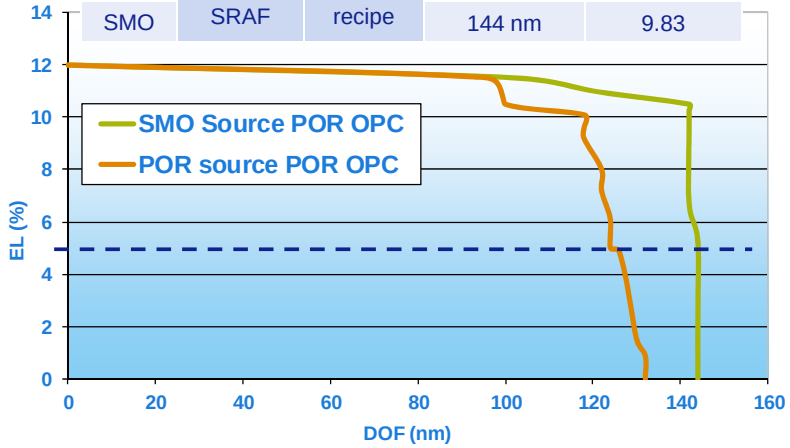


Figure 3. Process window comparison between POR source & SMO source with POR OPC

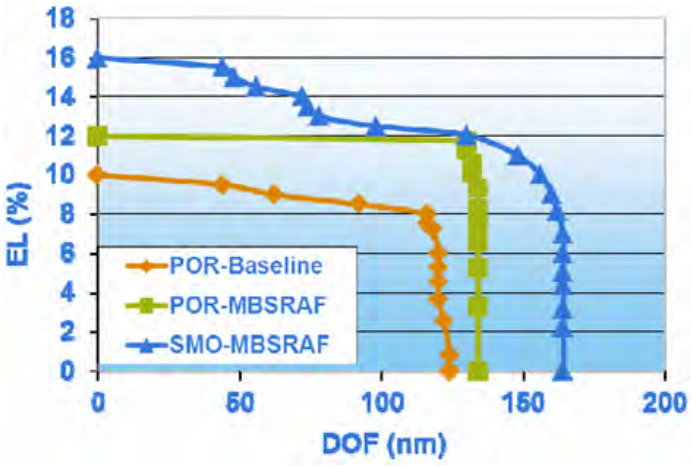
3.2 SMO Source verification with Class B

To verify the SMO source benefit, another set of test pattern Class B with more extensive weak point test patterns, was prepared. There were approximately 600 clips, including 500 process window sensitive weak points excluding the whole set of class A. As the goal was to verify the overall process window for all the test patterns, pattern selection would not be used and all the clips were used for process window characterization analysis.

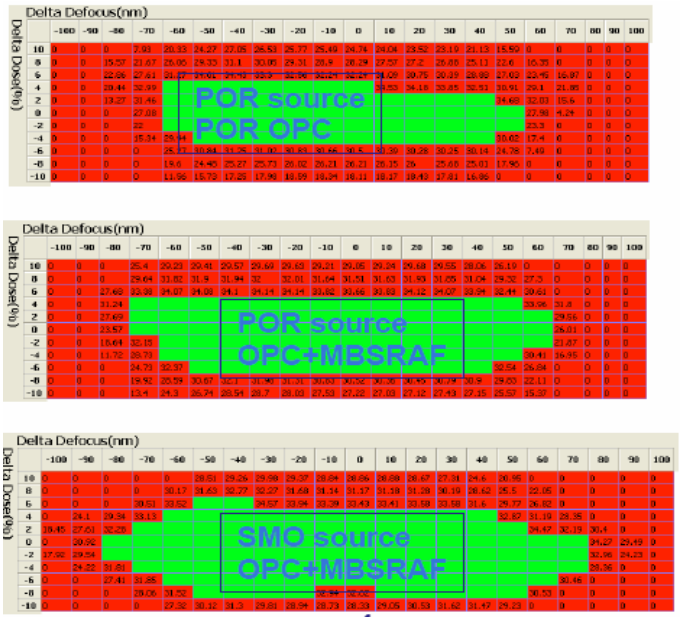
To understand the benefit achieved by the SMO source, 3 source-OPC splits were performed on Class B test structures: POR source with POR OPC, POR source with MB-SRAF OPC+ and SMO source with MB-SRAF OPC. The process window analysis results are shown in Figure 4. The DOF value in this experiment was based on LMC process window checking with a necking and bridging spec of 33 nm and 35 nm, respectively. The overlap DOF@5% EL of the SMO source was 166 nm, improved by 38% compared with the POR source with POR OPC. With the same mask optimization keyword, MB-SRAF OPC+, the DOF@5%EL for the SMO source was improved by 24%. The worst MEEF was also improved with the SMO source. Figure 4(b) was the DOF vs. EL plot for the 3 source-OPC splits from the OPC & LMC result. Figure 4(c) shows the process window tolerance based on the LMC catastrophic error spec, which demonstrated clearly that the SMO source achieved the biggest DOF among the 3 source-OPC splits. The worse PV-Band of the SMO source was improved from 27 nm to 24 nm, by 12%.

Source	Mask	DOF @ 5%EL	Worst MEEF
POR	Baseline OPC	120nm	13.19
POR	MB-SRAF OPC+	134nm	11.2
SMO	MB-SRAF OPC+	166nm	10.26

(a) DOF & worst MEEF for POR source & SMO source



(b) DOF vs EL plot for POR source & SMO source



(c) DOF from LMC result for POR source & SMO source

Figure 4. Process window comparison on Class B between POR source & SMO source

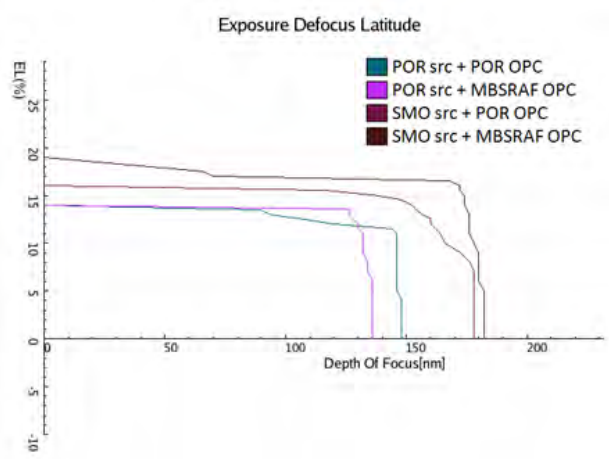
3.3 SMO Source verification with a larger-area device chip

Both class A and class B were the small sized test clips with a limited number of structures. For further SMO source verification, two critical real devices with larger-areas (790 um x 90 um) were chosen for hotspot check & process window analysis. In all 4 source-OPC splits were used for the comparison to extract the effects caused by source and OPC scripts: POR source with POR OPC, POR source with MB-SRAF OPC, SMO source with POR OPC, SMO source with MB-SRAF OPC.

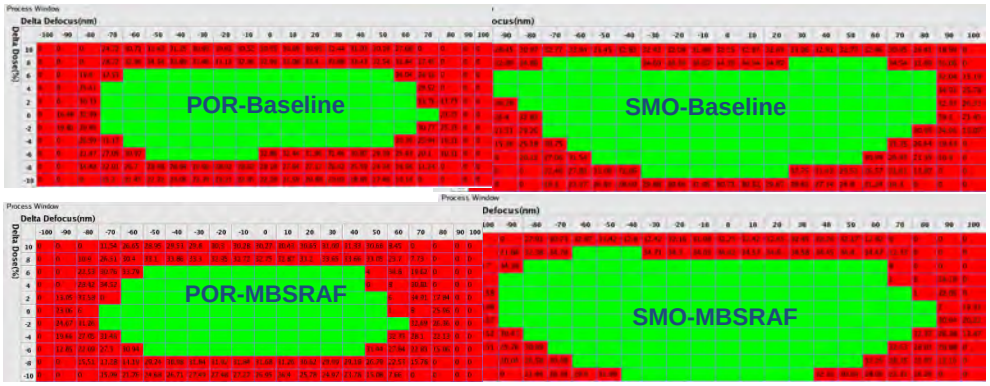
Figure 5 (a) shows the EL vs. DOF curves for the 4 source-OPC splits respectively. With EL = 5% the SMO source achieved larger DOF than the POR source, no matter which OPC scripts were applied, so the SMO source was the main contribution for the process window improvement. The SMO source with MB-SRAF OPC had a slightly better process

window than the SMO source with POR OPC. This was because the POR OPC script was optimized referenced to the POR source, not the SMO source. Figure 5 (b) shows the similar trend of the process window for the 4 source-OPC splits based on the LMC check result. The right two graphs shows the DOF result by SMO source with POR OPC and MB-SRAF OPC, which was apparently larger than the DOF shown from the left two graphs with the POR source.

Figure 5 (c) is the LMC result and process window characterization summary for the 4 source-OPC splits. Based on all of the criteria, including DOF, MEEF, hotspot number and catastrophic CD value, etc., the SMO source with MB-SRAF OPC achieved the best result. To extract the benefit gained from the MB-SRAF, we could focus on the comparison from the POR OPC split, which was used for the production mask generation. According to the columns 2 and 4 in the Figure 5 (c), DOF of the SMO source was around 166 nm, which was improved by 13.7%. The worst MEEF of the SMO source was also improved by 17.7%. The number of hotspots with the SMO source was reduced by 14.3% compared with the POR source. Both necking and bridging hotspot were improved simultaneously, and LEPB (Line End Pull Back) error was also eliminated with the SMO source.



(a) DOF vs. EL plot for POR source & SMO source



(b) DOF from LMC result for POR source & SMO source

Criteria	Spec		POR src + baseline OPC	POR src + MB-SRAF + OPC	SMO src + baseline OPC	SMO src + MB-SRAF + OPC
DOF	> POR		146 nm	132 nm	166 nm	178 nm
MEEF	< POR		11.12	12.47	9.15	9.15
Hotspots	Count Necking Bridge LEPB	< POR	1042 34.31 nm 34.90 nm 4.29 nm	1014 34.51 nm 34.95 nm 5 nm	893 35.00 nm 36.08 nm -	845 - 35.81 nm -

(c) LMC result and process window characterization summary for POR & SMO source

Figure 5. Process window comparison on large-area device between POR source & SMO source

4. WAFER VERIFICATION

Based on all the above data, the source verification based on simulation result showed that the SMO source has achieved an improved process window with increased DOF & EL and less MEEF. With OPC & LMC check on large area devices the number of hotspots was decreased and catastrophic CD values were improved with the SMO source. Since the benefits were proven based on simulation, it is more interesting to verify it on a real silicon wafer.

To eliminate the effect on process window benefit caused by OPC model accuracy and OPC recipe convergence, a new OPC model and OPC recipe with the new SMO source were calibrated and optimized, and a new mask was generated by launching the OPC keywords optimized for the SMO source. The work flow is shown in Figure 6. With the SMO source implemented on the scanner a wafer was printed and litho data with off-focus and off-dose condition was collected for the SMO model calibration. A 3 dimensional mask model (M3D) was calibrated with Tachyon FEM+, and the OPC recipes were optimized based on the SMO M3D model. A new SMO reticle was commissioned with the SMO source OPC split. By making a wafer with the new SMO reticle the process window benefit could be verified, to determine if it could be a good candidate to consider for production release.

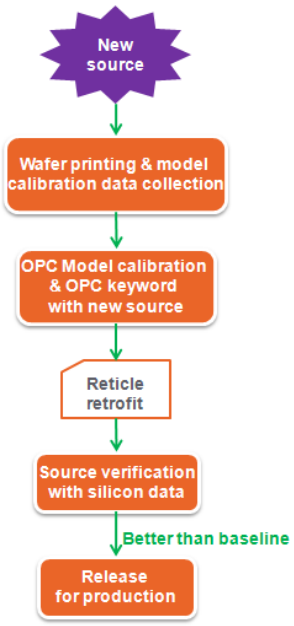
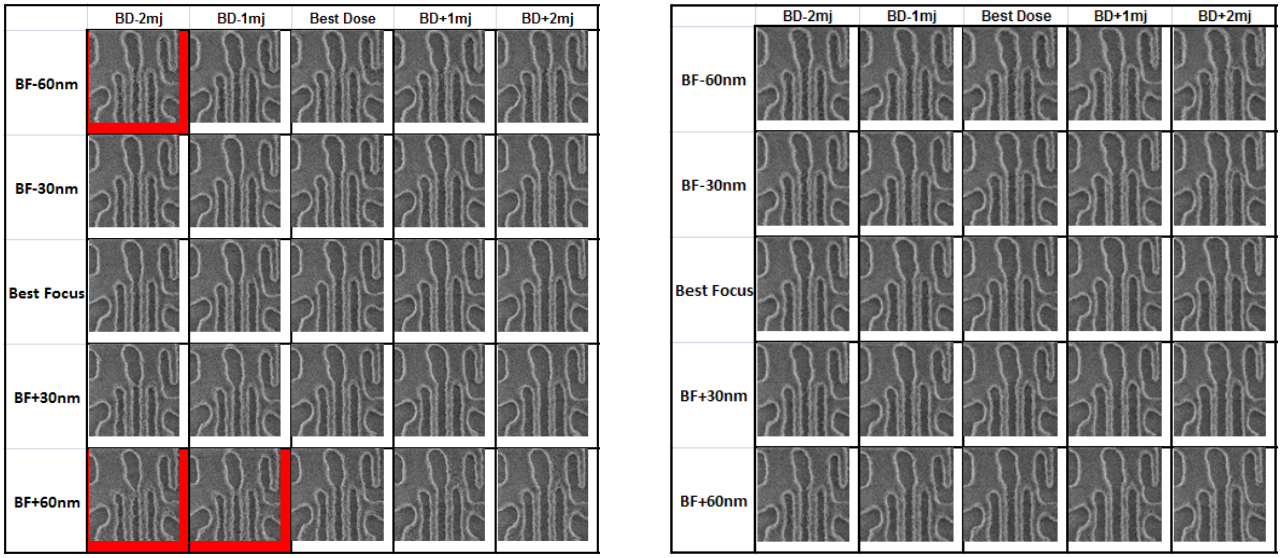


Figure 6. SMO wafer verification working flow

For comparison a POR FEM wafer was also printed on the POR reticle with POR source. Best focus and dose condition were determined separately based on the SMO FEM wafer data and POR FEM wafer data. The delta of the best focus between the SMO wafer and the POR wafer was around 10 nm and the delta of the best dose between the SMO wafer and the POR wafer was around 0.5 mJ/cm^2.

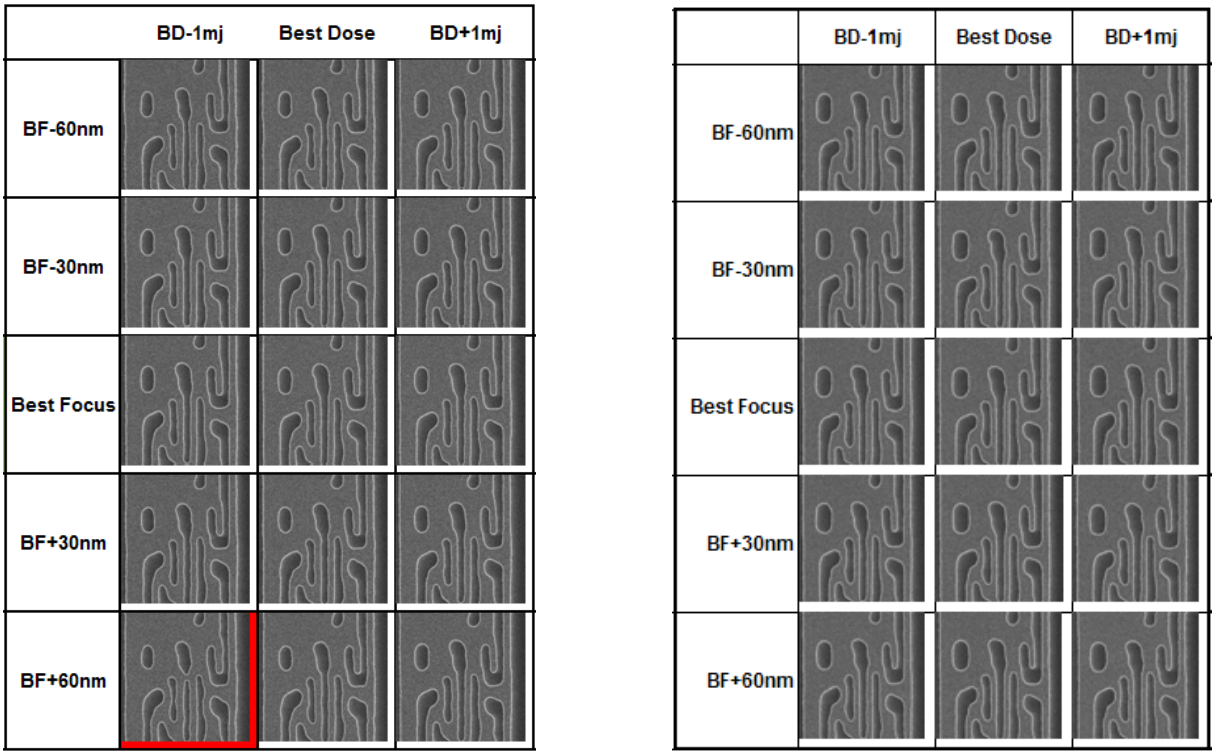
To verify the process window improvement gained from the SMO source, litho and etch data of the critical structures, such as weak points and electrical monitor structures, were measured with CD-SEM tool for both the SMO and the POR wafer. The wafer CD and SEM image were captured at nominal condition as well as off-focus and off-dose conditions. For a fair comparison, the same scanner for wafer printing and the same CD-SEM tool for wafer measuring were used, to avoid the differential factors caused by tools. Figure 7 is the litho SEM image of the hot spots for the POR wafer and the SMO wafer. The SEM image for the dose +/-1 mj, +/- 2 mj & defocus+/- 30 nm, +/- 60 nm were captured. For the POR wafer, when under-exposed by 2 mj, there was a serious necking error at defocus +60 nm. While with the SMO source, there was no defect observed at the same process window conditions. So based on this structure, pinching defect with POR source at 60nm defocus was resolved with SMO source. Lithographic process window with SMO source was improved compared with the POR.

The process window benefit from the SMO source could also be verified with the SEM image after etch, which is shown in Figure 8. Figure 8 (a) is the FEM SEM image after etch with the POR source and Figure 8 (b) is the FEM SEM image after etch with the SMO source. In Figure 8 (a) there is a hard necking error at defocus +60 nm with best dose -1 mj, and this is solved with the SMO source as show in Figure 8 (b). So the process window for both litho and etch process were improved with the SMO source.



(a) Litho FEM SEM image with POR source (b) Litho FEM SEM image with SMO source

Figure 7. SEM image after litho process for both POR source and SMO source



(a) FEM SEM image after etch with POR source (b) FEM SEM image after etch with SMO source

Figure 8. SEM image after Etch process for both POR source and SMO source

5. SUMMARY

The Tachyon Source Mask Optimization work flow and methodology to optimize an illumination source for use in a production environment was evaluated and verified. The diffraction-based pattern selection algorithm was demonstrated and proven to reduce SMO runtime significantly without compromising the process window performance. The pattern selection was proven to be robust as no iterations or use of the feedback loop to provide exceptions or hotspot clips back in to the source tuning was required. The benefits of the SMO source over the POR source can be realized through simulation using an extensive set of 500 process window sensitive weak points. The overlap DOF@5% EL of the SMO source was improved by 38% compared with the POR source with POR OPC. The SMO source was also effective to improve the worst MEEF. In addition the SMO source was verified with a larger-area device chip and was effective at improving the DOF (by 13.7%), the worst MEEF (by 17.7%) and reducing the number of hotspot (by 14.3%) as compared to the POR source. Necking and line-end pull back defects were eliminated with the SMO source.

The effectiveness of the Tachyon SMO source was verified on silicon. Necking defects with the POR source at 60 nm defocus were resolved with the SMO source. This shows that the SMO source can be applied on a full-chip level and was able to improve the lithography and etch process window without introducing new hotspots.

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